REMARKS

Applicant has carefully reviewed and considered the Office Action mailed on November 16, 2004, the references cited therewith, and the Decision on Appeal mailed on July 11, 2006. Claims 1-2, 7-8, 10, 15, and 17 are amended, no claims are canceled, and no claims are added; as a result, claims 1-21 remain pending in this application.

Reservation of Rights

Applicant does not admit that references cited under 35 U.S.C. §§ 102(a), 102(e), 103/102(a), or 103/102(e) are prior art, and reserves the right to swear behind them at a later date. Arguments presented to distinguish such references should not be construed as admissions that the references are prior art.

§103 Rejection of the Claims

Claims 1-2, 4-5, and 7-8 were rejected under 35 USC § 103(a) as being unpatentable over Gilbert et al.(U.S. 6,041,376) in view of Arimilli et al.(U.S. 6,138,218).

With regard to claim 1, the Office Action asserts that Gilbert *et al.* discloses "setting a status flag to indicate that a bus transaction is pending; and

retrying each subsequent nonmodifying bus transaction for the shared resource until the status flag is cleared."

A careful reading of Gilbert *et al.*, however, reveals that this assertion is incorrect, and the differences between Gilbert et al. and the claimed invention are even more apparent with respect to the clarifying amendments presented.

Gilbert et al. teaches using a hold flag to prevent other processors from accessing information on a node that another processor has already requested. (col. 2, ll. 43-50) Other processor requests are must be retried when any processor has a request for a particular node or resource that is first in time. (col. 3, ll 1-8) Regardless of whether the processor request is a read or a write, the procedure is the same. (col. 7, ll 5-10) In summary, according to Gilbert et al., all processor requests, reads, writes, or others, access a node on a first-come first-serve basis and the

first in time to access the resource may set a status flag to require subsequent processor requests to be retried. (col. 2, ll. 43-50; col. 7, ll. 5-10)

Applicant respectfully submits that the technique disclosed by Gilbert et al. does not solve the problem as disclosed by Applicant in the specification. In fact, Applicant describes a system such as the system of Gilbert et al. in the background section of the specification:

> However, certain architectures do not permit multiple bus transactions to be outstanding for a single shared resource. In these architectures, the processor that initiated the transaction "first" is allowed to complete the transaction. All subsequent transactions are retried if the transactions are for the same resource and the transactions occur before the first transaction has completed. A transaction may be retried any number of times until the transaction is allowed to complete. (p. 1, l. 29)

The live-lock problem which Applicant proposes to prevent is not solved by the system disclosed in Gilbert et al. The live-lock problem occurs when a read (a non-modifying bus transaction) is accessing a resource, and a write (a modifying bus transaction) attempts to access the resource. Gilbert et al. would allow the read to lock out the write. The processor requesting the read would then snoop the attempting write transaction and the requested data would be invalidated causing the reading processor to retry the read request. The reading processor, still in control of the resource, would begin reading again. The problem then occurs when the write request is subsequently retried. This causes the reading processor again to snoop the incoming transaction, causing the invalidation of the read data, and the cycle begins again. This cycle allows neither the read to finish reading nor the write to have access, and locks up the transactions and the resource. This is the live-lock scenario which is solved by the Applicant. Gilbert et al. does not address or solve this problem, as the first-come first-serve method of Gilbert et al. would nevertheless allow this live-lock problem to occur.

With reference to claim 1 as amended, the distinction from Gilbert et al. should be more apparent. Applicant solves the live-lock problem by identifying modifying transactions (e.g. write transactions) versus nonmodifying transactions (e.g. read transactions). Modifying transactions are allowed to set the status bit, indicating that a bus transaction is attempting to modify the resource. Nonmodifying transactions do not set the status flag, because as recited, the status bit indicates "that a bus transaction attempting to modify the shared resource is pending." When the status bit is set, by a bus transaction attempting to modify the resource, all

other bus transactions will be retried. This includes any current read transactions operating on the resource. Rather than providing first-come first-serve access to the resource, live-lock is prevented by allowing priority access to modifying bus transactions.

Additionally, the status bit indicates "that a bus transaction attempting" to modify, whereas both Gilbert et al. and Arimilli et al. disclose setting a status flag after the transaction already has the resource. By setting the flag on an attempt to modify, a modifying bus transaction can set the status flag and gain access to the resource even though a nonmodifying bus transaction already has the resource. By setting the flag on an attempt, the modifying bus transaction can set the flag even though another nonmodifying bus transaction has control of the resource.

Gilbert et al. describes when a hold flag is set at column 2, line 52-56 wherein, " In one aspect of the invention, a remote cache interconnect (also called a network controller) within a node has access to a hold flag. The remote cache interconnect sets or activates the hold flag when it receives data from the system interconnect for delivery to a requesting processor." Therefore, the hold flag refereed to in the Office Action is used by Gilbert et al. to indicate that a remote cache has received data, and not "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending," as recited in claim 1.

Further, Arimilli et al. at column 3, lines 5-12 states, "When a device snooping the system bus of a multiprocessor system detects an operation requesting data which is resident within a local memory in a coherency state requiring the data to be sourced from the device, the device attempts a intervention. If the intervention is impeded by a second device asserting a retry, the device sets a flag to provide historical information regarding the failed intervention." therefore, Arimilli et al. discloses setting a bit as a historical information regarding a failed intervention, and so fails to teach or suggest setting of a status bit to indicate that a bus transaction is attemmpting to modify either a shared resource as recited in claim 1 of the present invention.

Because neither Gilbert et al. nor Arimille et al., either alone or in combination, teach or suggest "setting a status bit to indicate that a bus transaction attempting to modify the shared resource is pending," or "retrying the first bus transaction and each subsequent nonmodifying bus transaction for the shared resource until the status bit is cleared" as recited in amended claim

1, the cited references fail to teach or suggest all the elements in the claim. Thus, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of obviousness with respect to claim 1. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 1.

With regard to claim 7, Applicant believes the arguments above regarding claim 1 generally apply to illustrate the disparity between the claimed invention and what is disclosed in both Gilbert et al. and Arimille et al. Additionally, claim 7 as amended recites with further clarity how the claimed invention does not follow the strict first-come first-serve process of Gilbert et al. Gilbert et al. does not describe any system where a bus transaction which has been granted a resource may be forced to retry as an incoming bus transaction steps in and sets a status flag to keep claim the resource or cache line.

Because neither Gilbert et al. nor Arimille et al., either alone or in combination teach or suggest all of the elements of claim 7. Specifically, Gilbert et al. and Arimille et al do not describe "setting a status bit to indicate that a bus transaction attempting to modify the cache line is pending;

retrying the first bus transaction if the status bit is set;

reissuing the second bus transaction that attempts to modify the cache line; and

granting the cache line for the reissued second bus transaction if the status bit is set for the cache line." Applicant believes this claim is patentable over Gilbert et al. and Arimille et al. Thus, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of obviousness with respect to claim 7. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claim 7.

Regarding claims 2, 4-5, and 9: Claims 2 and 4-5 depend from claim 1. Claim 9 depends from claim 7. For reasons analogous to those stated above and elements in the claims, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of obviousness with respect to claims 2, 4-5 and 9. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 2, 4-5, and 9.

Claims 3, 6, and 9 were rejected under 35 USC § 103(a) as being unpatentable over Gilbert et al.(U.S. 6,041,376) in view of Arimilli et al.(U.S. 6,138,218) as applied to claims 1 and 7 above and further in view of Donley et al. (U.S. 5,761,446).

Regarding claims 3, 6, and 9: Claims 3 and 6 depend from claim 1, and claim 9 depends from claim 7. Claims 3, 6, and 9 include all the elements of the independent claim from which they depend. For reasons analogous to those stated above and elements in the claims, Applicant respectfully submits that neither Gilbert et al. nor Arimilli et al. fail to teach or suggest all the elements of claims 3, 6 and 9. The Office Action relied on Donley et al. to supply these missing elements. Therefore Applicant submits neither Gilbert et al. nor Arimilli et al., nor Donely et al., alone or in combination recite all the elements of claims 3, 6, and 9. Hence, the Office Action fails to state a *prima facie* case of obviousness with respect to claims 3, 6, and 9. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 3, 6, and 9.

Claims 10-21 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Vogt et al. (U.S. 5,897,656) in view of Gilbert et al. (6,041,376).

Regarding Claims 10, 15 and 17: As amended, claims 10 and 15 each recite, "a status indicator associated with each one of the plurality of buffers, the status indicator being set to indicate that nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the shared resource" or "system memory." As amended, claim 17 recites, "a plurality of status indicators being set to indicate that nonmodifying bus transactions are to be retried when a modifying bus transaction attempts to access the one of the cache line." These claims, as amended further clarify the novelty of the present invention, and more visibly illustrate the differences between the references cited by the Examiner. The Office Action relies on Vogt et al. and Gilbert et al. The argument presented above regarding claim 1 with regard to Gilbert applies here. Additionally neither Gilbert et al. nor Vogt et al., either alone or in combination teach or suggest all of the elements of claims 10, 15 or 17. Specifically, at a minimum, neither reference describes the elements presented above in this paragraph.

The Applicant believes claims 10, 15 and 17 are patentable over Gilbert et al. and Vogt et al. Thus, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of obviousness with respect to claims 10, 15 and 17. Accordingly, Applicant requests reconsideration, withdrawal of the rejection, and allowance of claims 10, 15 and 17.

Regarding Claims 11-14, 16, and 18-21: Claims 11-14, 16, and 18-21 depend from independent claims 10, 15, and 17 respectively, and therefore include all the elements of the independent claim from which they depend. For reasons analogous to those stated above and elements in the claims, Applicant respectfully submits that the Office Action fails to state a *prima facie* case of obviousness with respect to claims11-14, 16, and 18-21. Therefore, Applicant requests withdrawal of the rejections and reconsideration and allowance of claims 11-14, 16, and 18-21.

Documents Cited but Not Relied upon for this Office Action

Applicant need not respond to the assertion of pertinence stated for the references cited but not relied upon by the Office Action since these references are not made part of the rejections in this Office Action. Applicant is expressly not admitting to this assertion and reserves the right to address the assertion should it form part of future rejections.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 349-9592 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: MS Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 11 day of September, 2006.

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